REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated March 31, 2003.

By the present amendment, independent claims 7 and 14 have been amended to clarify the invention. In addition, new claims 43-50 have been added to further define the invention in terms of further features and defining the invention in means plus function format.

Briefly, the present invention is directed to an improved arrangement for manufacturing devices having high reliability gate oxide films for peripheral circuit MOS transistors in nonvolatile semiconductor memory devices such as, for example, flash memories.

As discussed with regard to Fig. 18 showing a sectional illustration of a prior art structure, memory cell devices such as flash memory have typically been comprised of a memory cell region in a peripheral circuit region in the manner shown in Fig. 18. More specifically, referring to Fig. 18, it can be seen that an interpoly insulating film 208 is located between a control gate 209 and the floating gate 207 of the memory cell transistors. The gate insulating films 210 of the peripheral circuit transistors, on the other hand, are formed of silicon oxide formed by the thermal oxidation method, as discussed, for example, on page 2, lines 22 and 23 of the specification. It has become common to use shallow groove isolation for the isolation between the peripheral MOS transistors for purposes of miniaturizing the elements, as discussed on page 3, line 19 et seq. of the specification.

Unfortunately, a number of problems have developed with the prior art structure, as discussed on pages 3-6 of the specification. In the first place,

Received from < 703 312 6666 > at 9/30/03 7:18:55 PM [Eastern Daylight Time]

Applicant's studies have revealed a degradation in silicon oxide formed gate oxide films of the peripheral circuit transistors. In addition, particularly when the shallow groove isolation technique is used, a "kink" tends to develop in the current-voltage characteristics of the high voltage transistors of the peripheral circuit. This tends to undesirably lower the breakdown voltage for those peripheral transistors. This phenomenon is discussed, for example, on page 3, line 13 through page 4, line 4.

An illustration of the "kink" in the current-voltage characteristics due to the characteristic degradation is shown in Fig. 3 and discussed, for example, on page 16, line 22 et seq. As noted there:

> "In the case of prior art using thermal oxidation method, a bump called kink was observed in the current/voltage characteristics, indicating characteristic degradation of the device."

In order to resolve these problems, especially the problem of the kink in the current-voltage characteristics of the high voltage transistors, Applicant has developed a device which uses a deposited silicon oxide film to form the gate insulators of the peripheral circuit transistors rather than a thermally oxidized film. Referring to Fig. 1F of the drawings, an example of this is shown by the nitrogen introduced silicon oxide film 108 which is first deposited over both the memory cell portions and the peripheral circuit portions of the substrate (e.g. see page 14, line 9 et seq.).

Turning to Fig. 2A, it can be seen that the portion of the silicon oxide layer 108 found in the memory cell region and the low voltage region of the peripheral circuit is then removed, leaving the deposited insulating film 108A only in the high voltage region of the peripheral circuit. Next, as shown in Fig. 2B, another nitrogen introduced silicon oxide layer 109 is formed over the memory circuit portion to serve as the interpoly dielectric film between the floating gate and the control gate. In

Received from < 703 312 6666 > at 9/30/03 7:18:55 PM [Eastern Daylight Time]

addition, the nitrogen introduced second deposited silicon oxide film 109 extends over the first deposited silicon oxide layer 108A. Thus, the second deposited silicon oxide insulating film 109 and the first deposited silicon oxide film 108A both serve to form the gate insulating films for the high voltage transistors of the peripheral circuit regions.

A close-up of the difference in structure between the prior art and this feature of the invention regarding the gate insulating film for the high voltage peripheral circuit transistors can be appreciated by studying Fig. 5A and 5B. As shown in Fig. 5A, the prior art utilizes a thermally oxidized oxide film 200 adjacent the shallow groove isolation area 102. This serves to create an area as shown by the circle E where the isolation is significantly reduced in thickness compared to the remaining portion of the thermally oxidized layer 200. In the present invention, as shown in Fig. 5B, on the other hand, by virtue of using the two deposited silicon oxide films 108A and 109A, the thickness for the isolation in the circled area E adjacent to the shallow groove isolation region 102 remains substantially constant. This difference, such as shown in Figs. 5A and 5B, between the present invention and the prior art serves to eliminate the kink in the current-voltage characteristic for the high voltage transistors, as shown in Fig. 3. This, in turn, substantially increases the breakdown voltage for these high voltage devices, as shown in Fig. 4 as compared with the thermally oxidized prior art devices.

Reconsideration and allowance of amended independent claims 7 and 14 over the cited prior art set forth in the 35 U.S.C. § 103 rejection based on Cappelletti (USP 6410387), Shum (USP 6327182) and He (USP 6143608) is respectfully requested. By the present amendment, each of the independent claims 7 and 14 has been amended to clearly define the structure of the present invention including:

Received from < 703 312 6666 > at 9/30/03 7:18:55 PM [Eastern Daylight Time]

1. A first deposited insulating film which is deposited on the semiconductor substrate to serve as at least one of the gate insulating films for the second (third) MOS field effect transistors in the peripheral circuit;
2. The interpoly dielectric film being comprised of a second deposited insulating film deposited on the floating gates; and
3. The second deposited insulating film also being deposited on the peripheral circuit region "to comprise at least a portion of the gate insulating films of the second MOS field effect transistors.

In other words, both independent claims 7 and 14 clearly define the use of first and second deposited insulating films to form the gate insulating films for the second (third) MOS field effect transistors in the peripheral circuit region, with the interpoly dielectric film also being comprised of a portion of the second deposited insulating film deposited on the floating gates.

It is respectfully submitted that Cappelletti, whether considered alone or in combination with the secondary references to Shum and He, completely fails to teach or suggest these features of the first and second insulating films deposited in the manner set forth in the present amended claims. In the first place, although the structure shown in Fig. 20 of Cappelletti appears to be somewhat similar to the presently claimed invention set forth in claims 7 and 14, it is respectfully submitted that there is nothing in Cappelletti that teaches or suggests that the insulating films in questions are actually deposited insulating films rather than thermally oxidized insulating films. For example, Fig. 20 show two low voltage high performance transistors at the right side with an oxide layer 3 which can be considered as corresponding to the second MOS field effect transistors and gate insulating films of

Received from < 703 312 6666 > at 9/30/03 7:18:55 PM [Eastern Daylight Time]

the present invention. In addition, two high voltage transistors are shown on the left side with a gate oxide layer 24, which can be regarded as corresponding to third MOS field effect transistor with the second gate insulating film in claim 14, for example. However, Cappelletti simply discloses oxide layers 3 and 24 formed on the substrate without defining the specific formation method for these layers. This is clear, for example, from column 3, lines 23-27 and column 4, line 64 though column 5, line 4. These portions simply discuss the formation of the films, but do not specifically teach or suggest that these are deposited insulating films rather than thermally oxidized films. The significance of the difference between using deposited silicon oxide films and thermally oxidized silicon oxide films is clearly explained in the specification with regard to Figs. 3, 4, 5A and 5B of the specification, as discussed above. Summarizing on this point, the use of thermally oxidized silicon oxide layers leads to the significant variation and insulator thickness, particularly when a shallow groove insulating structure is being used, as shown in Fig. 5A. This leads to the kink shown in the Fig. 3 in the current-voltage characteristics of the high voltage devices, as well as the reduced breakdown for such devices shown in Fig. 4. The recited use of deposited films and the claimed relationships between the first and second deposited films overcomes these problems.

Beyond this, both the amended claims 7 and 14 define:

> "wherein said second deposited insulating film is also formed on said peripheral circuit region to comprise at least a portion of the gate insulating films of the second MOS field effect transistors." (Claim 7)

Claim 14 defines a similar feature. As such, both claims 7 and 14 clearly that the same second deposited insulating film used to form the interpoly insulating film over the floating gates in the memory cell portion is used as at least a portion of the gate

Received from < 703 312 6666 > at 9/30/03 7:18:55 PM [Eastern Daylight Time]

insulators for the peripheral cell transistors. It is respectfully submitted that Cappelletti completely fails to teach or suggest this feature.

More specifically, referring to Fig. 7 of Cappelletti, the dielectric layer 18 formed on the gate electrodes 8 and 9 of the high voltage transistors is shown on the left side of the drawings. As such, the dielectric layer 18 is not used as either the oxide layer 3 of the high voltage transistor or as the gate oxide layer 24 of the low voltage high performance transistor. As such, unlike the present invention where the second deposited layer is used both for the interpoly dielectric layer and part of the gate insulator for the high voltage peripheral cell transistors, no such second deposited layer for these two purposes is provided in Cappelletti. Still further, neither Shun nor He at all suggest anything which would lead to modifying Cappelletti to arrive at these claimed features. Therefore, reconsideration and allowance of amended claims 7 and 14 is earnestly solicited.

Reconsideration and allowance of the dependent claims 43 and 44 is also respectfully requested. These claims particularly define the structures such as shown in Fig. 2B of the present application and Fig. 5B in which the first and second deposited films are used in conjunction with one another as a multiplayer structure for forming the gate insulator of the high voltage peripheral circuit transistors. This serves to even further define over the arrangement taught by Cappelletti, whether considered alone or in combination with He and Shum.

Consideration and allowance of new independent claims 45 and 47 and their respective dependent claims is also respectfully requested. Independent claims 45 and 47 define the invention in terms of "means for preventing a kink in the current-voltage characteristics of the second (third) MOS field effect transistors of the peripheral cell region." The means is specifically defined in terms of the use of the

Received from < 703 312 6666 > at 9/30/03 7:18:55 PM [Eastern Daylight Time]

OCT 0 1 2003 OFFICIAL

first and second deposited silicon oxide layers in the manner discussed above. As such, new independent claims 45 and 47 define a particular functioning means to prevent a problem which is not even addressed in any of the cited prior art. As such, it is urged that these independent claims 45 and 47, together with their respective dependent claims, even further define over the cited prior art which is quite unconcerned with the problem of the kink in the current-voltage characteristics of peripheral cell transistors. Therefore, reconsideration and allowance of these claims is also earnestly solicited.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 500.39879X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Reg. No. 28,141

GEM/dlt

1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Telephone: (703) 312-6600
Facsimile: (703) 312-6666

Received from < 703 312 6666 > at 9/30/03 7:18:55 PM [Eastern Daylight Time]